Datasheet

AS1135

13W/30W 802.3af/at (Draft2.0) PoE Powered Device with Integrated DC-DC Controller

Revision 1.0, March 2008

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GENERAL DESCRIPTION

The AS1135 is a single-chip, highly integrated CMOS solution for Power over Ethernet (PoE) Powered Devices requiring input power of up to 30Watts. Applications include Voice over IP (VoIP) Phones, Wireless LAN Access Point, Security Cameras, WiMax Terminals, Point of Sales Terminals, RFID Readers, Thin Clients and Notebook computers.

The AS1135 integrates input Surge Protection, a PD controller, and a low-emission DC-DC controller. The AS1135 implements all the physical layer Powered Device (PD) functionality as required by the IEEE802.3af-2005 and IEEE802.3at (Draft 2.0) standards. This includes 2-event classification, Type2 PSE detection indicator (AT-Detect) in addition to PD detection, under-voltage lockout, and hot-swap FET integration.

The AS1135 has been architected and designed to address both EMI emission concerns and surge/over-voltage protection in POE applications. The AS1135 implements many design features that minimizes transmission of system common-mode noise on to the UTP. On-chip integration of surge protection provides faster ressponse to surge events and limits stray surge current from passing through sensitive circuits, such as the Ethernet PHY device. The device is designed to provide a safe low impedance discharge paths directly back to the earth ground, resulting in superior reliability and circuit protection.

By using high-volume standard CMOS technology, Akros enables its customers to implement higher performance PoE devices with low cost and a small footprint.

FEATURES

The AS1135 is fully integrated and architected at a system level to provide the following features:

- Fully supports *IEEE*® Std. 802.3af-2005 and supports pre-standard *IEEE*® Std. 802.3at (Draft 2.0) power requirements
- Supports "two event" classification for pre-standard IEEE® Std. 802.3at (Draft 2.0) higher power PD applications
- Provides Type 2 PSE detection per 802.3at standard (Draft 2.0)
- Meets IEC 61000-4-2/3/4/5/6 requirements for EMC Compliance
- Meets IEC 60950 isolation requirements
- Integrated DC-DC controller, provides exceptional EMI performance
- Programmable DC current limit up to 800mA
- Provides seamless support for local power down to 10V
- Low Rds-on hot-swap FET (typical 0.8Ω)
- Over temperature protection
- Industrial temperature range, -40°C to +85°C
- 5x5 mm, 20 lead QFN Package, RoHS compliant

TYPICAL APPLICATIONS

- Pan, Tilt and Zoom (PTZ), Security and Web Cameras
- Voice over IP (VoIP) phones
- Wireless LAN Access Points, WiMax Terminals
- Point of Sale (PoS)Terminals, RFID Terminals
- Thin Clients and Notebook Computers
- Fiber to the Home (FTTH) Terminals

EXAMPLE APPLICATION

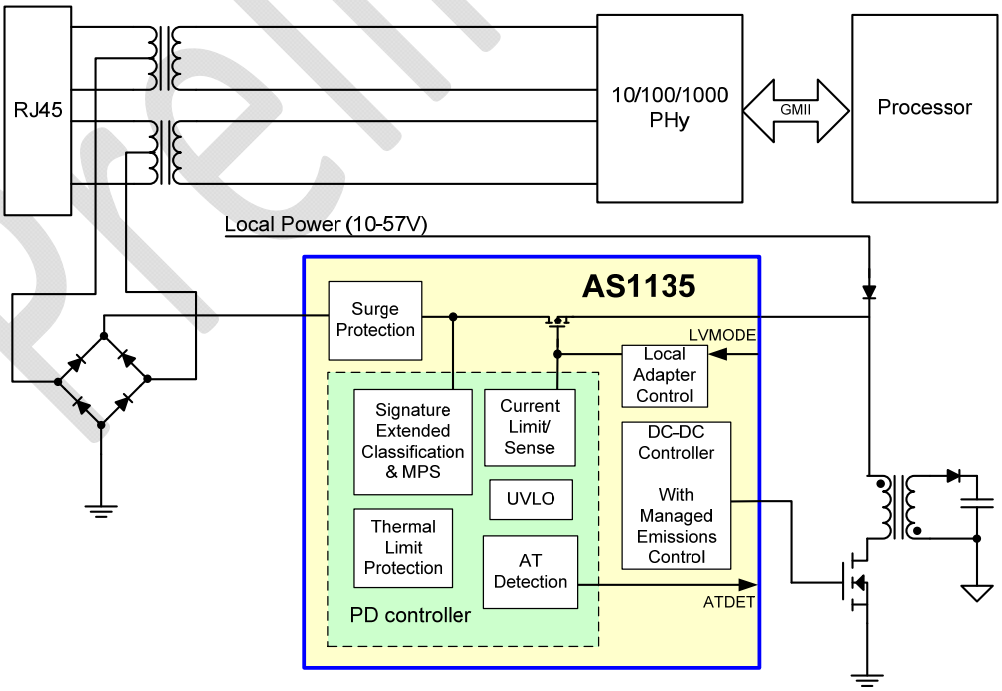


Figure 1: Typical Application Diagram for a PoE PD (Flyback Converter)

PIN-OUT DIAGRAM

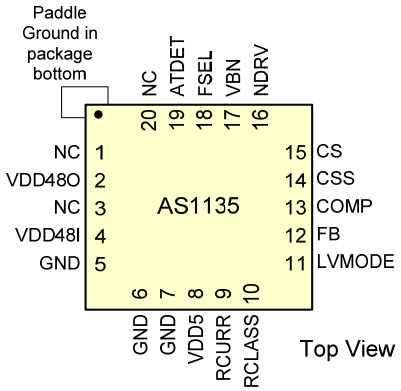


Figure 2: Pin-out Diagram

PIN DESCRIPTIONS

Table 1. Pin Assignments

Pin	I/O	Name	Description
1	-	NC	No Connect
2	P	VDD48O	Switched 48V supply output
3	-	NC	No Connect
4	P	VDD48I	48 V bus pin. This pin is the positive bus fed by the output of the external diode bridge. The bus requires the connection of a detection signature capacitor (100nF) and detection signature resistor (26.7kΩ)
5	A	GND	Must be connected to paddle ground (GND).
6	A	GND	Must be connected to paddle ground (GND).
7	A	GND	Must be connected to paddle ground (GND).
8	O	VDD5	Internal 5 volts bus decoupling point
9	A	RCURR	Current limit pin. Connection to paddle ground sets the current limit to 400mA (for 13W applications). Open circuit sets the current limit to 800mA (for 30W applications).
10	A	RCLASS	Classification resistor connection
11	A	LVMODE	Local Voltage Mode. When pulled high, LVMODE opens the internal FET switch and keeps the DC-DC controller active. This is a current mode input pin. Please see description for usage details. .
12	A	FB	DC-DC Controller feedback point
13	A	COMP	DC-DC Controller error amplifier compensation network connection
14	A	CSS	DC-DC Controller soft-start capacitor connection point
15	A	CS	DC-DC Controller peak current sense input (low side)
16	O	NDRV	DC-DC Controller N-MOSFET gate drive
17	O	VBN	DC-DC Controller low side supply decoupling
18	I	FSEL	Frequency Select. This pin sets the switching frequency of the DC-DC converter
19	O	ATDET	802.3at PSE detect. High level output indicates availability of higher system power, either via connection to a Type 2 PSE for pre-802.3at, or via Local Power supply
20	-	NC	No Connect
Paddle	P	GND	Local analog ground. This is the negative output from the diode bridge, and is not isolated from the line input

Key:

I = Input **A = Analog signal**

O = Output **P = Power**

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings[1]

Description	Max Value	Units
High voltage pins (4—VDD48I; 2—VDD48O)	60	Volts
Low voltage pins (8—VDD5; 9-RCURR; 10—RCLASS; 11—LVMODE; 12—FB; 13—COMP; 14—CSS; 15—CS; 16—NDRV; 17—VBN; 18—FSEL; 19—ATDET)	6	Volts
ESD Rating:		
Human body model[2]	2	kV
ESD charged device model	500	V
ESD Machine Model	200	V
System level (contact/air) at RJ-45[3]	8/15	kV
Temperature		
Storage Temperature	165	°C
Junction Temperature	150	°C

[1] Absolute maximum ratings are limits beyond which damage to the device may occur.

[2] The human body model is as described in JESD22-A114.

[3] System ESD testing done per IEC61000-4-2.

NORMAL OPERATING CONDITIONS

Table 3. Normal Operating Conditions

Unless otherwise noted, specifications are for V_{in} = 48V.

Description	Min	Typical[1]	Max
V_{in}	36V	48V	57V
Operating temperature range,	-40°C		+85°C

[1] Typical specification; not 100% tested. Performance guaranteed by design and/or other correlation methods.

KEY ELECTRICAL CHARACTERISTICS

Table 4. Electrical Characteristics

Unless otherwise noted, specifications are for Ta = -40°C to +85°C and VIN = 48V (at RJ45 input).

	Min	Typical[1]	Max	Units	Comments
PD Section					
Inrush Current Limit		200		mA	For Vin>30V during startup
Max. operating current – Type 1	375	400	500	mA	Pin 9 (RCURR) pulled to GND; device configured for 13W operation
Max. operating current – Type 2	TBD	750	TBD	mA	Pin 9 (RCURR) left open; device configured for 30W operation
Switch On Resistance, R_{DS-ON}		0.8	TBD	Ω	
Reset voltage level	0		2.7	V	
Min Detection Signature voltage			2.7	V	
Max Detection Signature voltage	10.1			V	
Min Classification voltage			14.5	V	In classification, the AS1135 sinks current as defined in Table 7
Max Classification voltage	20.5			V	
Min Mark Event Voltage			6.9	V	
Max Mark Event Voltage	10			V	
Mark Event Current	0.25		2	mA	When the input voltage is less than Vmark_th Min during the classification signature, type 2 PD must draw mark event current
Mark Event Threshold	10		14.5	V	
Classification Reset Threshold	2.8		6.9	V	
ATDET high		4.7		V	
ATDET low		0		V	
Full power activation threshold			42	V	
Full power de-activation threshold	30			V	
DC-DC Controller Section					
F_{OSC} (SMPS) switching frequency	100	350	500	kHz	DC-DC Controller operating frequency, selected by Rosc resistor, 1%
Fosc tolerance		±10%			
F_{OSC} Temperature Coefficient		0.12		%/C	
NDRV R_{OUT}		1.2	3	Ω	Output drive resistance
Gate Drive Dynamic Response NDRV T_R, T_F		2.2 2		nS nS	10% - 90% with C_{Load} = 1 nF
V_{PK}, peak current sense threshold voltage at CS	460	600	700	mV	Ipeak=Vpk/Rsense
Max. duty cycle		80		%	Internally limited
Min. duty cycle		6		%	Internally limited
VBN		4.7		V	Internal supply voltage; sets V_{OH} of NDRV.
Error amplifier reference voltage	1.45		1.55	V	Compared to input of the FB pin
Soft start ramp time		2		ms	Conditions: CSS=100nF
COMP source current		30		µA	FB = 0V, COMP=0V

Table 4. Electrical Characteristics

Unless otherwise noted, specifications are for Ta = -40°C to +85°C and VIN = 48V (at RJ45 input).

	Min	Typical[1]	Max	Units	Comments
COMP sink current		30		µA	FB = 5V, COMP=5V
Open loop voltage gain		80		dB	
Small signal unity gain bandwidth		5		MHz	COMP connected to FB.
FB leakage (source or sink)		1		µA	0V>FB>4.5V
Local Power Mode					
LVMODE Threshold Low (I_{il})	20			uA	
LVMODE Threshold High (I_{ih})			80	uA	
Local Power Operating Voltage Range	10		57	V	Local power applied between VDD48O and GND, using LVMODE feature. Note that power transformer must be capable of handling that full voltage range
Thermal Protection					
Thermal shutdown temperature		165		°C	Above this Temp., the AS1135 is disabled.
Max. on-die operating temperature		140		°C	
Current reduction temperature threshold		145		°C	Temperature at which thermal current reduction is applied
Thermal current reduction		50		%	
Thermal current reduction hysteresis		20		°C	Temperature change required to restore full operation after thermal current reduction
Thermal shutdown hysteresis		40		°C	Temperature change required to restore full operation after thermal shutdown

[1] Typical specifications are not 100% tested. Performance guaranteed by design and/or other correlation methods.

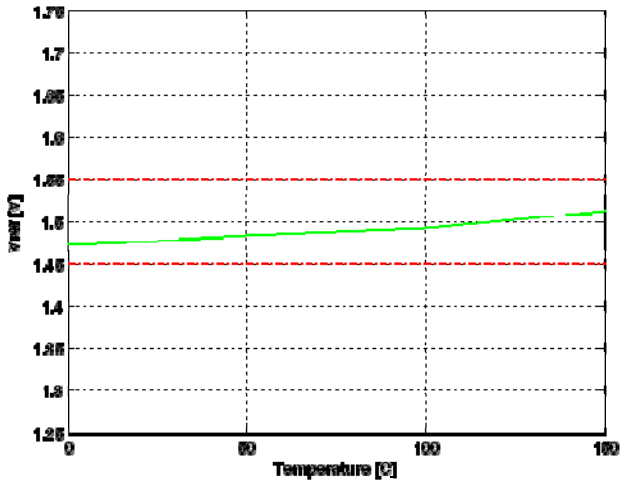
Table 5. Package Thermal Characteristic

	Min	Typical[1]	Max	Units	Comments
Thermal Resistance, Junction to Ambient, θ_{JA}		31		°C/W	20 lead QFN package
Thermal Resistance, Junction to Case, θ_{JC}		3.4		°C/W	20 lead QFN package
Power dissipation, P_{DISS}		0.9		W	25W output (12V output at 2.5A)

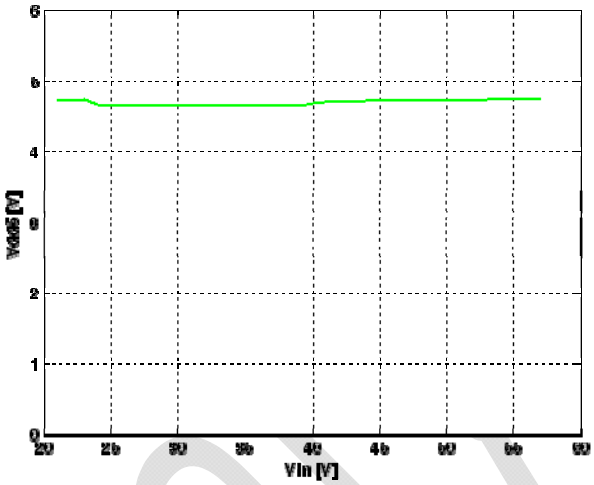
[1] Typical specifications are not 100% tested. Performance guaranteed by design and/or other correlation methods.

TYPICAL PERFORMANCE CHARACTERISTICS (PRELIMINARY)

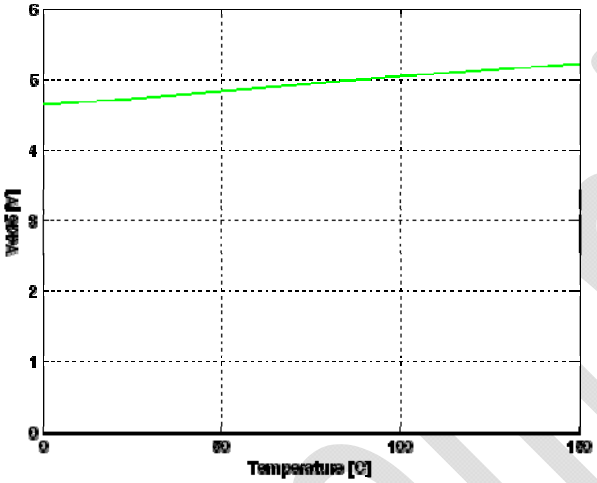
Feedback Error Amplifier VREF vs. Junction Temp



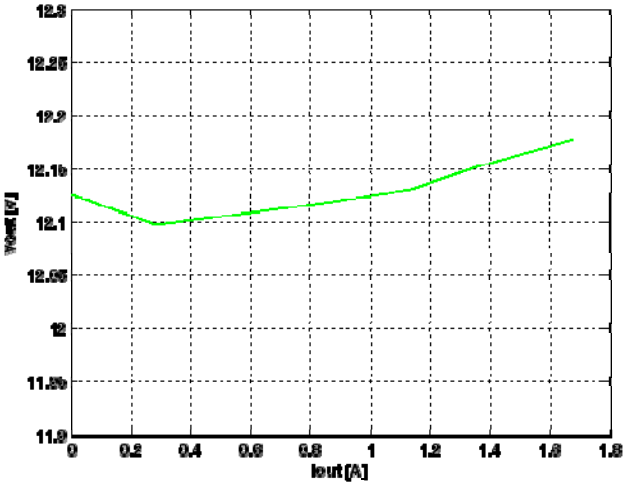
VDD5 vs. Vin



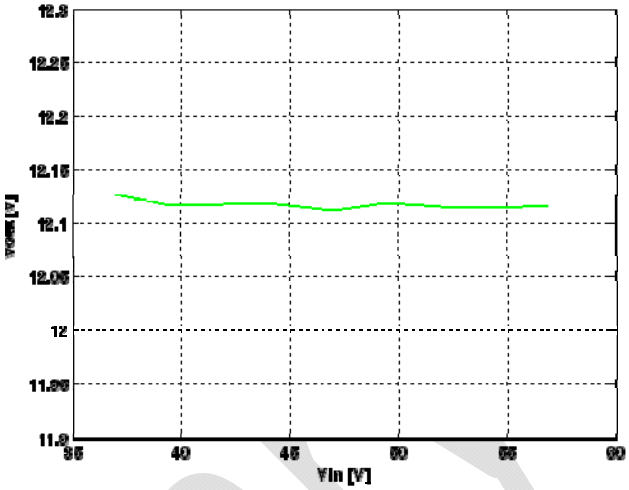
VDD5 vs. Junction Temperature



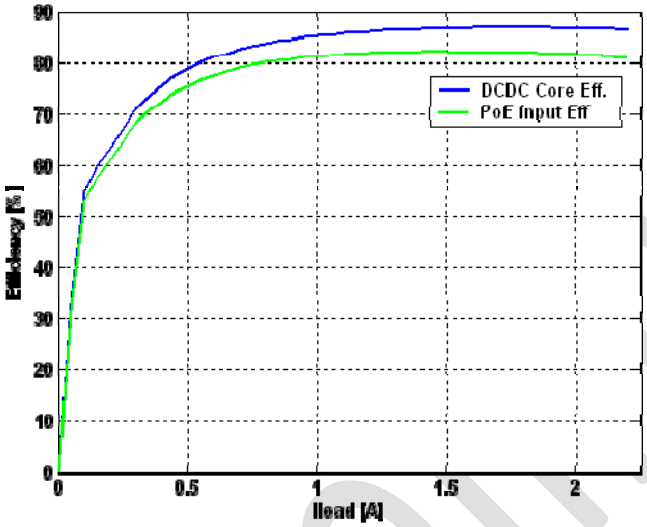
DCDC Load Regulation vs. IOUT @ VIN=48V, VO = 12V



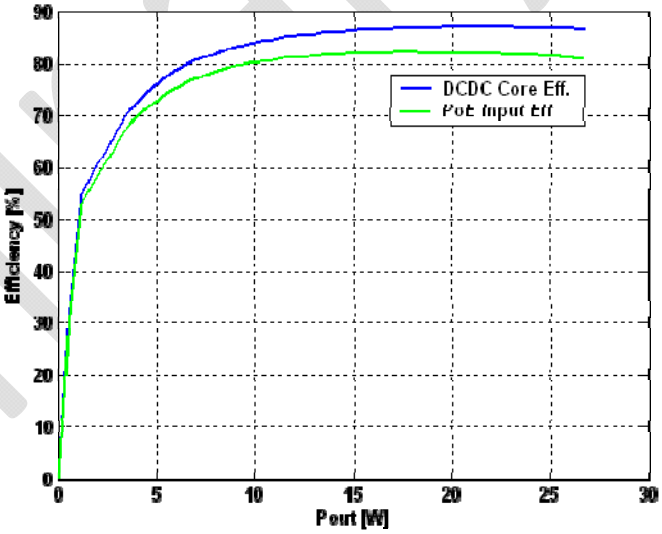
DCDC Line Regulation @ IOUT=0.25A, 12V



DCDC Efficiency vs. IOUT @ VIN=48V, VO = 12V



DCDC Efficiency vs. POUT @ VIN=48V , VO = 12V



FUNCTIONAL DESCRIPTION

OVERVIEW OF POE

Power over Ethernet (PoE) offers an economical alternative for powering end network appliances such as IP telephones, wireless access points, security and web cameras, and other powered devices (PDs). The PoE standards *IEEE*® Std. 802.3af and 802.3at are intended to standardize the delivery of power over the Ethernet cables in order to accommodate remotely powered client devices. These standards define a method for recognizing PDs on the network and supplying different power levels according to power level *classes* with which each PD is identified. By employing this method, designers can create systems that minimize power usage, allowing more devices to be supported on an Ethernet network.

The end of the link that provides power through the Ethernet cables is referred to as the power sourcing equipment (PSE). The powered device (PD) is the end of the link that receives the power. The standard defines as Type1 PD or Type1 PSE that is designed for IEEE Std. 802.3af-2005 power levels (<13W at the PD input). A Type 2 PD or Type2 PSE that is designed for greater than IEEE Std. 802.3af-2005 power levels (>13W at the PD input).

The PoE method for recognizing a PD and determining the correct power level to allocate uses the following sequence:

- *Reset*, wherein power is withdrawn from the PD if the applied voltage falls below a specified level.
- *Signature Detection*, during which the PD is recognized by the PSE.
- *Classification*, during which the PSE reads the power requirement of the PD. The Classification level of a PD identifies how much power the PD requires from the Ethernet line. This permits optimum use of the total power available from the PSE. (Classification is considered optional by *IEEE*® standard 802.3af-2005. But IEEE® standard 802.3at (Draft 2.0) requires Type 2 PSE to classify PD for mutual identification.)
- *ON* operation, during which the allocated level of power is provided to the PD.

This sequence occurs as progressively rising voltage levels from the PSE are detected.

To design PoE systems according to the PoE standard, designers have the following constraints:

Table 6. PoE Requirements

Requirement	Value
Maximum Type 1 PD input power	12.95W
Maximum Type 2 PD input power	29.5W
Output voltage from Type 1 PSE	44-57V
Output voltage from Type 2 PSE	50-57V
Minimum of operating current limit Type 1 @ PSE min output voltage	350mA
Minimum of operating current limit Type 2 @ PSE min output voltage	720mA
Line resistance (for Type 2 operation)	12.5 Ω
Input voltage at Type 1 PD interface	37V-57V
Input voltage at Type 2 PD interface	41V-57V

AS1135 PoE DESIGN

To help designers meet these requirements, the AS1135 is a fully integrated PoE PD controller for Type1 and Type2 PD implementations. The AS1135 meets all system requirements for the *IEEE*® 802.3 standard for Ethernet and all power management requirements for *IEEE*® standard 802.3at (Draft 2.0).

The AS1135 acts as an interface to the PSE, performing all detection, classification, and inrush current limiting control necessary for compliance with the PoE standards. An internal MOSFET and control circuit limits the inrush and steady-state current drawn from the Ethernet line. External diode bridges protect against polarity reversal, to provide alternative A and B detection. The AS1135 passes 8kV Contact Discharge and 15kV Air Discharge tested per IEC 61000-4-2. EMI compliance of AS1135 based design has been verified for CISP22 and FCC Class-B radiated emissions and conducted emissions.

POWER FEED ALTERNATIVES FOR 10/100/1000 SYSTEMS

PSE supplies power to single link PoE PD. PSE located in the Data Terminal Equipment or Repeater is called endpoint PSE, while PSE located between MDIs is named as Mid-span PSE. Figure 3 illustrates the two power feed options allowed in the 802.3af/at(pre) standard for 10/100/1000 systems. In Alternative A, a PSE powers the end station by feeding power along the twisted pair cable used for the 10/100/1000 Ethernet signal via

the center taps of Ethernet transformers. On the line side of the transformers for the PD, power is delivered through pins 1 and 2 and returned through pins 3 and 6. In Alternative B, a PSE powers the end station by feeding power through pins 4, 5, 7and 8. In 10/100/1000 system, this is done through the center taps of Ethernet transformer. In a 10/100 system using Alternative B, power is applied directly to the spare cable pairs without transformers.

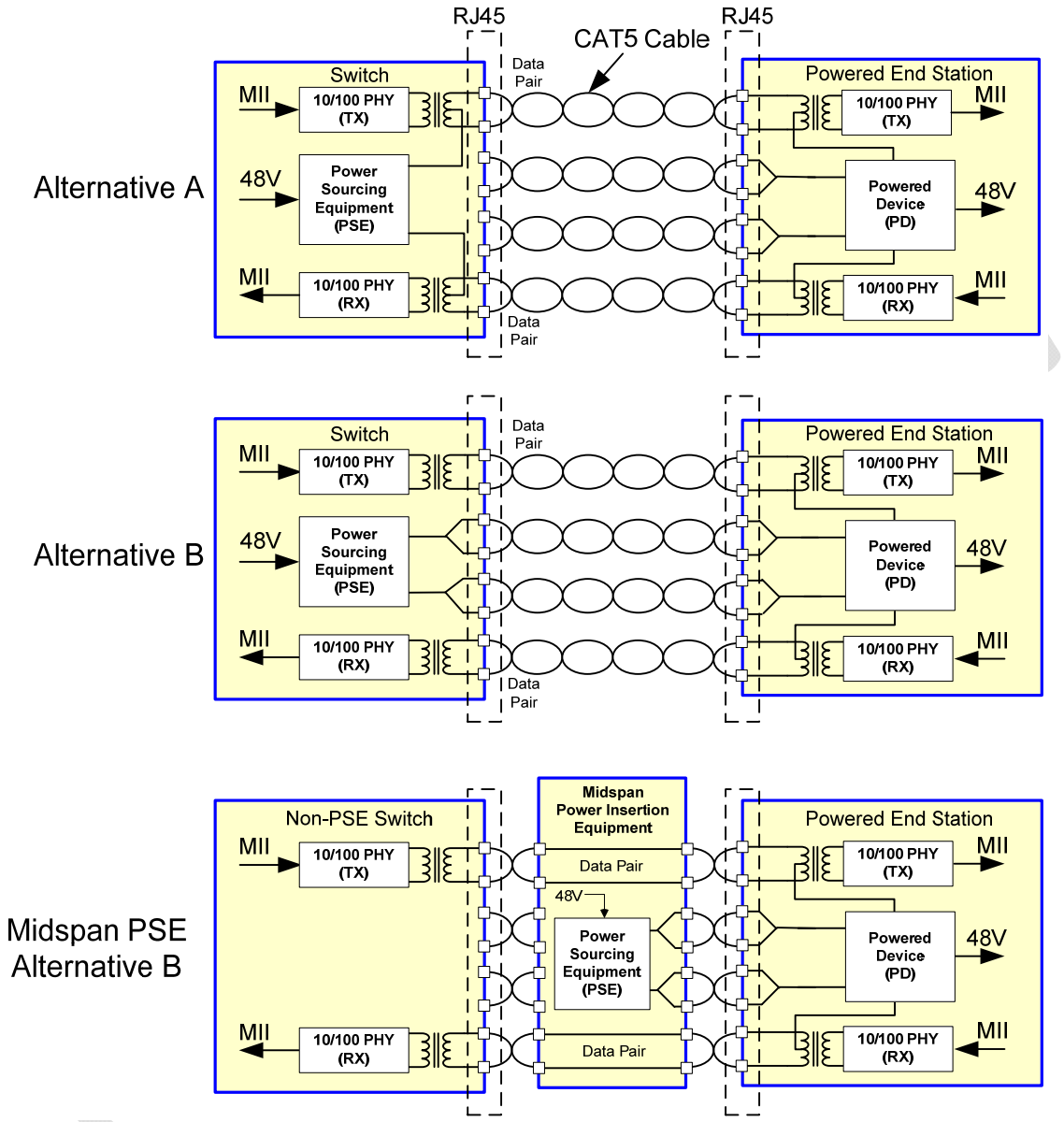


Figure 3: IEEE® Std. 802.3af-2005 Power Feeding Schemes for 10/100 Systems

The *IEEE*® Std. 802.3af/at are intended to be fully compliant with all existing non-powered Ethernet systems. As a result, the PSE is required to detect via a well-defined procedure whether or not the connected device is PD compliant and classify the needed power prior to applying power to the system. Maximum allowed voltage is 57V to stay within SELV (Safety Extra Low Voltage) limits.

AS1135 OVERVIEW

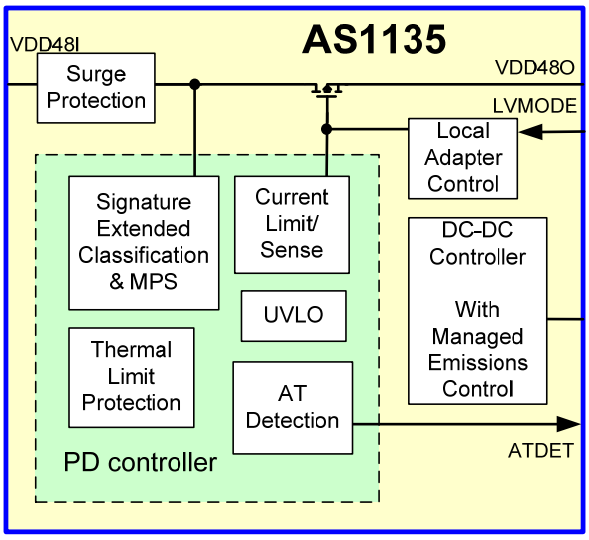


Figure 4: Top-Level Block Diagram of the AS1135

The AS1135 is a fully integrated PD that provides the functions required for Power-over-Ethernet (PoE) applications. The optimized architecture of the AS1135 reduces external component cost in a small footprint while delivering high performance.

RECTIFICATION & PROTECTION

To protect against polarity reversal external diode bridges are required. In conjunction with the external diode bridge, the AS1135 includes over voltage and transient protection on the line side of the hot-swap FET.

By integrating protection circuitry, Akros has produced a solution that provides a much faster response to surge events. The design limits stray surge current from passing through sensitive circuits, such as the Ethernet PHY device and enables a low impedance safe discharge paths directly back to the earth ground. The protection circuit itself is carefully designed to ensure that during these surge events, where currents can sometime be as high as 30A, that voltages do not exceed critical breakdown and spark gap limits so they themselves are not destroyed by the event.

PD CONTROLLER

The AS1135 PD Control interface is designed to provide full PD functionality for IEEE 802.3af and 802.3at (Draft 2.0) compliant systems, with programmable support for the standard PD control functions.

The PD Controller provides the following major functions:

- Provides a resistance/capacitance for detection signature.
- Provides classification currents for power classification.
- Provides PD full power.
- Manages power and thermal protection overrides, including UVLO (under voltage lockout).
- Provides an ATDET signal when connected to a Type 2 PSE that can deliver more than 13Watts to the PD
- Provides 2-event physical layer classification
- Provides Maintain Power Signature feature

Modes of Operation

The AS1135 has five operating modes:

1. Reset—the classification state machine is reset, and all blocks are disabled.
2. Detection —The PD detection signature resistance / capacitance is applied across the input.
3. Classification—PD indicates power requirements to the PSE via a single event classification for 802.3af or through 2-event Physical Layer classification as 802.3at (Draft 2.0).
4. Idle—This state is entered after classification, and remains here until full-power input voltage is applied.
5. ON—The PD is enabled, and supplies power to the DC-DC controller and the local application circuitry.

As the supply voltage from the PSE increases from 0V, the AS1135 transitions through the modes of operation in this sequence:

Reset ⇨ Signature Detection ⇨ Classification ⇨ Idle ⇨ ON

If no PSE or local power supply is present, line voltage will be zero and that will hold the AS1135 in the reset state. The AS1135 does not affect the Ethernet link function.

Reset

When the voltage supplied to the AS1135 drops below the minimum valid detection voltage (i.e. <2.7V), the chip will enter the reset state. In the reset state, the AS1135 consumes very little power, the power supply to the PD is disconnected, and conditions revert to pre-classification.

Detection Mode

During detection mode, the PSE applies a voltage to the AS1135 PD to read its detection signature. The reading of the signature determines whether or not a PD is present and, if so, allows the PSE to determine the power class the PD belongs to.

To detect a PD, the PSE applies two voltages—1V or more apart—in the detection voltage range (2.7V to 10.1V) and extracts a detection signature resistance value from the I-V slope. Valid resistance (I-V slope) values are between 23.75kΩ and 26.25kΩ. For the AS1135, detection signature resistance is generated by an external resistor between VDD48I and GND. Typically this is a 26.7kΩ, 1% resistor.

Valid PD also presents valid detection signature capacitance (0.05~ 0.12uF @ 2.7V to 10.1V), and reasonable offset voltage (1.9V) per the 802.3af/at standard, measured at the PD input connector. AS1135 detection signature capacitance is generated by an external 0.1uF capacitor between VDD48I and GND. The offset voltage is mainly determined by the external diode bridge voltage drop.

Classification Mode

Each class represents a power allocation level for a PD, so that PSE can manage power between multiple PDs. *IEEE*® Std. 802.3at (Draft 2.0) defines classes of power levels for PDs as shown in Table 7. The AS1135 supports 2-event physical layer classification per *IEEE*® Std. 802.3at (Draft 2.0) as shown in Figure 5.

AS1135 identifies the PSE type as either Type 1 or Type 2. If the 2-event method is successfully detected by the PD controller during the classification stage it asserts the ATDET pin high, indicating connection to a Type 2 PSE. If the PD controller detects only single-event classification, it identifies the PSE to be Type 1 and ATDET pin is asserted low.

If a PSE is Type 1, to classify the AS1135, the Type 1 PSE presents a voltage between 14.5V and 20.5V to the PD and determines its class by measuring the load current the PD sinks.

If a PSE is Type 2, in order to classify the AS1135 as the Type 2 PD, AS1135 has to be set as Class 4, so that AS1135 returns a class-4 signature.

The AS1135 allows the user to program the classification current via an external resistor in the RCLASS pin. Current, power levels and programming resistor values for each class are shown in Table 7.

Use the following equation to determine typical classification current:

- $$I_{CLASS}[mA] = 2.0 + \frac{2360}{R_{CLASS}[k\Omega]}$$
- Tolerance = Maximum of ±1.8mA or ±9%
- R_{CLASS} > 63.4kΩ

Table 7. Classification Settings

Class	Power (W)	Iclass (mA)	Rclass (kΩ)
0	0.44-12.95	0-4 mA	Pull-up, 1%
1	0.44-3.84	9-12 mA	280kΩ, 1%
2	3.84-6.49	17-20 mA	143kΩ, 1%
3	6.49-12.95	26-30 mA	90.9kΩ, 1%
4	12.96 –29.5	36-44 mA	63.4kΩ, 1%

Idle Mode

In the Idle mode, between Classification and the ON state, PD Current is limited to monitoring circuitry to detect the on-state threshold.

ON State

In the ON state, the AS1135 is supplying power.

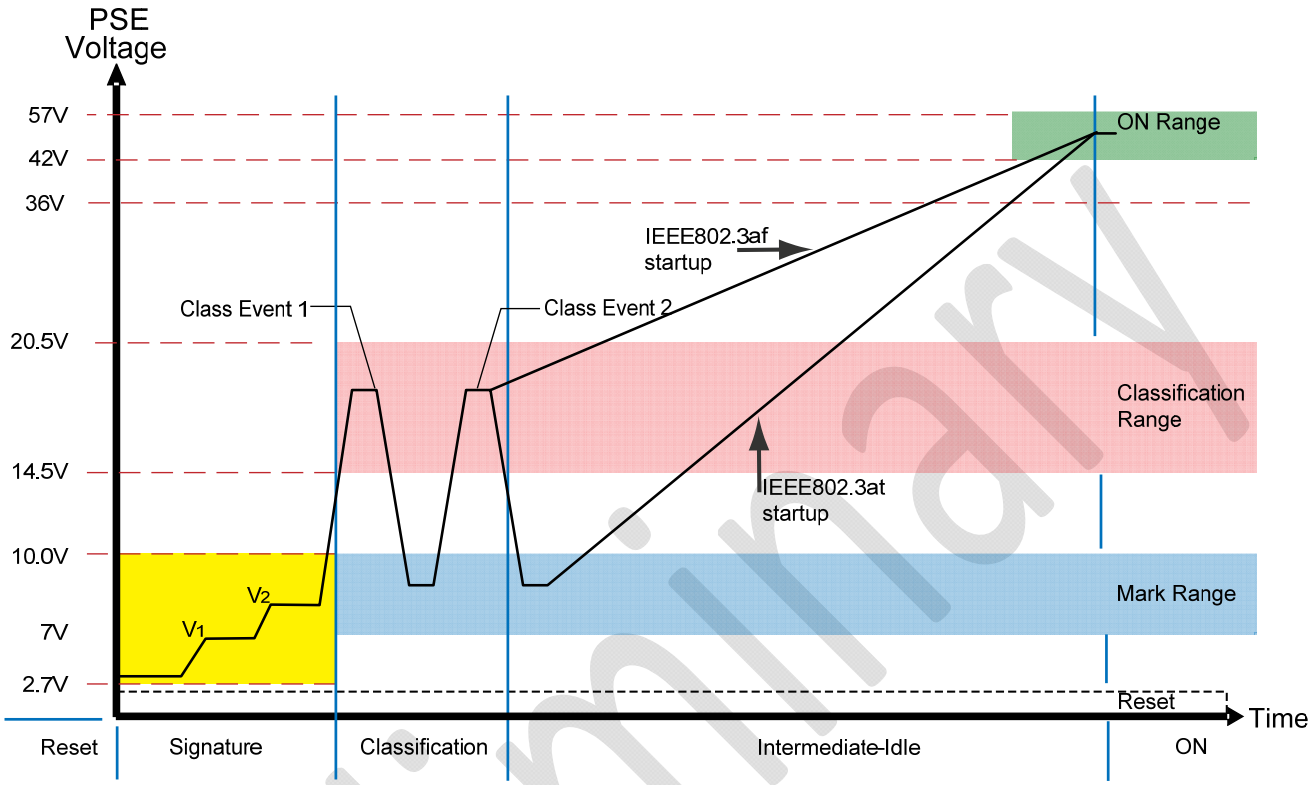
At a voltage at or above 42V, the PD turns on and full power is available via the AS1135 DC-DC Controller.

Maintain Power Signature (MPS)

PSE requires PD to provide Power Signature in order to maintain supply power to the PD. The AS1135 provides internal circuit to maintain at least 10mA of DC current to present the maintain power signature to the PSE. At no load or starting up stage, the PD consume minimum of 10mA. Once proper load is established at the DC-DC converter output stage, the PD internal load circuitry for MPS is turned off to reduce the total chip power consumption.

PoE Power-On Startup Waveform

Figure 5 represents the power-on sequence for PoE operation. The waveform reflects typical voltages present at the PD-PI during signature, classification and power-on.



Notes

1. Voltages V1 and V2 are applied by a PSE to extract a signature resistance value.
2. The PSE takes current readings during Class Events to determine the class of the PD. At this time, the PD presents a load current determined by the resistance on the RCLASS pin.
3. After the PSE measures the PD load current, if it is a high power PSE it presents a mark voltage (between 7V and 10V) followed by a second classification. The PD responds by presenting a load current as determined by the resistor on the RCLASS pin. After the PSE measures the PD load current the second time, and determines that it can deliver the requested power, it moves into the ON state by raising the voltage above 42V.

Figure 5: 802.3at (Draft 2.0) Typical Power-On Waveform

PD CONTROLLER POWER AND THERMAL PROTECTIONS

The AS1135 provides the following PD controller power and thermal protections:

- Under Voltage Lockout (UVLO)
- Current Limit with integrated current sense
- Thermal Limit/Protection

Under Voltage Lockout (UVLO)

The AS1135 contains a line Under-Voltage Lockout (UVLO) circuit. The UVLO circuitry detects conditions when the supply voltage is too low (less than 30V), and disconnects the power to protect the PD.

Inrush Current Limit/Current Sense

Inrush limiting maintains the cable voltage above the turn-off threshold as the input capacitor charges. Also, it helps prevent the PSE from going into current limit mode. The Current Limit/Current Sense circuitry also minimizes PD on-chip temperature peaks by limiting inrush current and operating current. It monitors the current via an integrated sense circuit and regulates the gate voltage on an integrated low-leakage 80V power MOSFET. In addition, the power MOSFET can be shut down by the PD Controller subsection or the Thermal Limit Protection subsection or local power adapter insertion while LVMODE pin 11 is pulled high.

Thermal Limit Protection

The AS1135 provides thermal protection for itself by monitoring die temperature and reducing maximum current or disconnecting power as needed to prevent pre-set thermal limits from being exceeded.

Two-stage thermal current limiting is implemented, which reduces the operating current limit by 50% when the die temperature reaches 145˚C, and disables the power MOSFET switch above 165˚C. Normal current limits in both cases are reapplied when the die temperature returns to 125˚C.

ATDET PIN

The ATDET output pin provides an indicator when higher than 13W of power is available to the system, either via link to a Type 2 PSE, or via use of Local Power Supply using the LVMODE feature. This pin can be used to directly drive an LED indicator and can also be used by the PD system controller to self-configure the PD based on available power.

If there is no Local Power, ATDET pin stays low during the PD Reset, Detection and Classification phases. The ATDET pin will be set high once the PD recognizes completion of the 2-event Physical Layer Classification as initiated by a Type 2 PSE. The pin will remain high and be reset to zero after the occurrence of a RESET (VDD48I < 2.77V) or a power-down event. ATDET pin remains low if it identifies the PSE partner to be Type 1 during the classification phase.

In case LVMODE is used to supply local power, the ATDET pin is set high irrespective of the PD mode. Please see Table 8 below for ATDET output definition under various powering modes.

Table 8. Truth Table of ATDET

ATDET signal status	PSE	
	Type 1	Type 2
LVMODE = Low	Low	High
LVMODE = High	High	High

LOCAL POWER MODE (LVMODE)

The LVMODE pin can be used in applications where the PD appliance draws power from either the Ethernet cable or an external DC local power adapter. The LVMODE pin is a current input pin with low and high thresholds as defined in the parametric Table 4. The LVMODE is in ON state when the input current going into the pin exceeds the I_{ih} threshold of the pin, and is in OFF state when the input current going into the pin is below the I_{il} threshold. If LVMODE operation is not desired, LVMODE pin should be connected to GND.

Figure 6 below shows simplified internal implementation and the external application circuit required to use the LVMODE feature. When local power is applied at the local adapter input, the AS1135 will enter the LVMODE mode. That will open the internal FET switch while the DC-DC converter remains operational. In this configuration, the local power input always gets the priority even in presence of the PoE power, irrespective of relative voltages. If the local power is removed, the device will exit the LVMODE operation and the PoE power can be used if available.

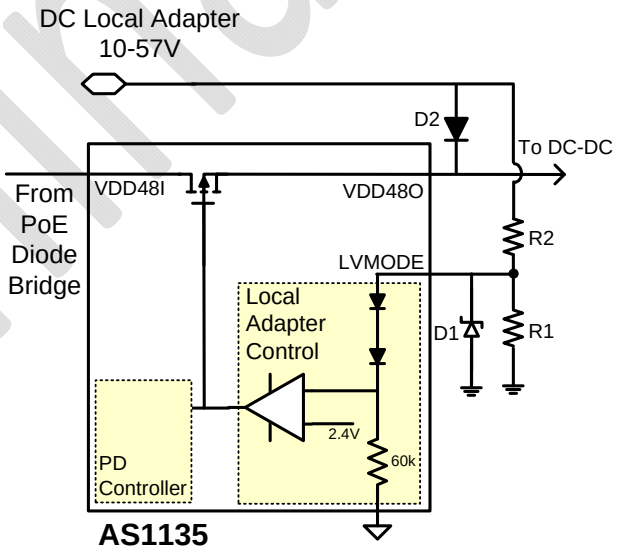


Figure 6: LVMode Implementation

The auxiliary power is injected at the VDD48O node through an external diode D2. For D2, use of a low reverse leakage diode (<350uA at worst case temperature) is recommended. This ensures that when there is no local adapter voltage, the PoE voltage at VDD48O does not falsely pull up the LVMODE pin due to high reverse leakage of the D2 diode. Please see Table 9 for appropriate part number information.

Appropriate ratio of R2 and R1 resistors can be used to ensure proper operation across all supply voltages. Table 9 shows appropriate choice of R2 and R1 resistors to work with variety of popular local adapter DC voltages. Though a common value of R2 and R1 can be used across the whole range of local supply voltage from 10V-57V, using different values per the table below minimize the power consumption. The maximum input voltage at the

LVMODE pin should not exceed 6V. A zener diode (D1) is recommended to limit the voltage at the LVMODE pin.

Since input current at the LVMODE pin defines the state of the part, it's recommended not to drive any other circuits or components directly from the LVMODE node (like LED) that may draw current. Additional indicators or current absorbing components may be driven directly from the Local Supply pin.

The internal DC-DC controller in AS1135 is designed to operate with input voltages ranging from 10V to 57V to allow applications to take benefit of the LVMODE feature. Besides configuring the device for LVMODE operation, the external power transformer must also be designed to ensure proper operation across the complete input range.

Table 9. LVMODE Configuration

Local Voltage Range	Recommended for Local Adaptors	R2	R1
10V-57V	12V, 18V	2.74kΩ	4.02kΩ
20V-57V	24V, 30V	11.3kΩ	4.02kΩ
32.4V-57V	36V, 48V	20kΩ	4.02kΩ

Diode D1: 5.6V Zener, BZT56V

Diode D2: S3B (100V/3A, worst case reverse leakage <250uA), use of low-reverse leakage diode with worst case reverse leakage under high temperature <350uA is recommended

DC-DC CONTROLLER

Overview

The DC-DC architecture is a current-mode controller which can be configured with external component changes to flyback, forward, or buck topologies. Both non-isolated and isolated topologies are supported.

As part of full system level solution for EMI, Akros has focused significant effort in reducing switching noise in the integrated power converters through unique techniques of shaping the FET drivers and reducing ground bounce by minimizing the dV/dt switching noise.

The integrated DC-DC controller operates from a switched input voltage (VDD48O) and includes soft-start and current limiting. Once input power is applied and enable signals are asserted, the DC-DC controller starts up. The controller provides gate control signal (NDRV) to external switching MOSFET, and uses an external resistor to sense the transformer primary current.

The DC-DC controller includes programmable soft start, 80% maximum duty cycle, programmable switching frequency and a true voltage output error amplifier.

Programmable PWM Frequency

The FSEL pin allows the DC-DC converter switching frequency to be set externally. Placing a resistor between FSEL and GND will set the nominal oscillator frequency. Table 10 identifies the resistor values for common switching frequencies.

Table 10. PWM Switching Frequency Selection

Switching Frequency (kHz)	FSEL Resistor (kΩ, 1%)
100	178
350	53.6
400	46.4
500	36.5

Current-Limit/Current Sense

The DC/DC controller provides cycle-by-cycle current limiting to ensure that transformer primary current limits are not exceeded. In addition, the maximum average current in the transformer primary is set by internal duty cycle limits.

Low Load Current Operation

The internal circuitry detects a low output power condition and puts the DC-DC Controller into a discontinuous current operation (DCM) mode.

Compensation and Feedback

For isolated applications, loop compensation and output voltage feedback is generally provided by an opto-isolator circuit, and

the FB pin is shorted to ground. In these applications, the COMP pin is pulled up to 4.8V (nominally) by an internal current source. This pull-up can be the termination for an opto-isolator, or an additional resistor can be used in parallel.

For non-isolated applications, a resistive divider network senses the output voltage and is applied directly to the FB pin. The internal error amplifier is connected to a 1.5V reference voltage and the control loop will servo the FB pin to this voltage. A capacitive/resistive network connected to the COMP pin provides loop compensation.

Soft-Start inrush current limit

The internal circuitry automatically ramps up the inrush current by limiting the maximum current allowed in the transformer primary magnetizing inductance per clock cycle. The amount of time required to perform a soft start cycle is determined by the CSS capacitor. A CSS capacitor of 330nF provides approximately 7ms of soft startup ramp time.

DC-DC CONVERTER TOPOLOGIES

Isolated Topologies

The DC-DC controller can be configured in several different isolated. The FLYBACK mode is chosen when a minimum number of external components is desired or there is a large step-down and the output voltage is < 7V. The FORWARD mode is chosen when lower switching noise is desired. Either of these isolated topologies can be designed for synchronous or non-synchronous operation, based on the system requirements. A reference schematic for High Efficiency Isolated Synchronous Flyback design is shown in Figure 8.

Non-Isolated Topologies

The BUCK mode is used in non-isolated applications. This application uses inductor for energy storage, instead of a transformer. The Buck designs have the smallest overall footprint. Figure 9 shows the BUCK converter in a non synchronous operation, where the output voltage is referenced to VDD48O. Since the FB voltage is ground referenced, the feedback signal must be level shifted back down to ground. This is accomplished by the two PNP transistors and the associated resistors.

THERMAL DE-RATING AND BOARD LAYOUT CONSIDERATIONS

The AS1135 is capable of operating to industrial temperature range of 85 ºC, in ambient air and without forced cooling. A thermal pad on the underside of the package dissipates heat generated by the PD die. In 30W applications, designers must consider thermal design as an integral part of their systems design and remove heat via this pad.

If the PCB landing pattern is properly designed, the QFN package should exhibit a thermal resistance of Θ_{JA}=31°C/W.

For adequate heat dissipation, the board layout must include a ground pad which accomplishes both the ground connection and dissipates the heat energy generated by the PD. Thermal vias are used to draw heat away form the PD package and to transfer it to the backside of the system PCB

The recommended PCB layout for the AS1135 is shown in Figure 7 below.

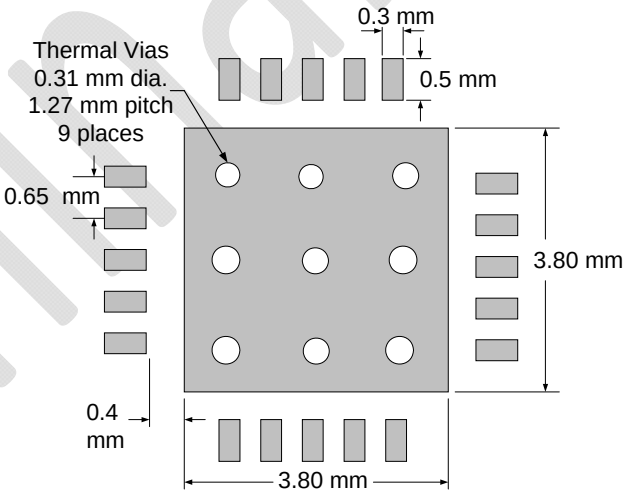
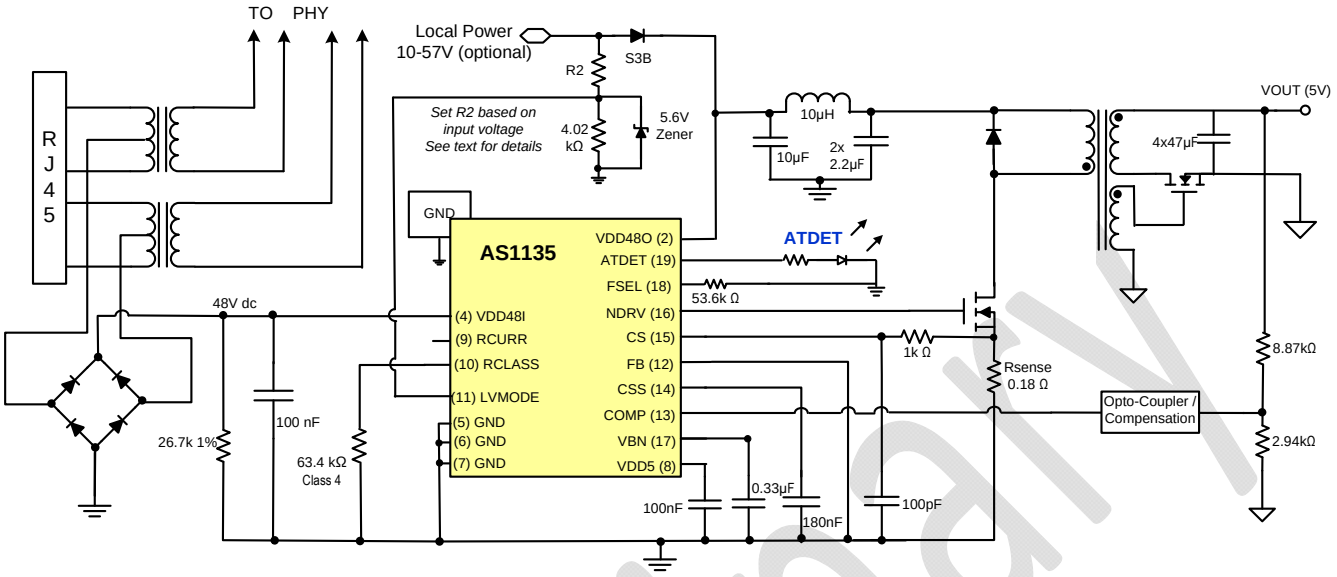


Figure 7: AS1135 PCB Footprint

APPLICATION CIRCUITS

Figure 8: PoE PD Controller with High Efficiency Isolated Synchronous Flyback DC-DC Converter (Conceptual Schematic)



Notes:

This is a simplified conceptual schematic. Please refer to the reference design documentation for detailed design and component information. Full PoE implementation will require 2 input diode bridges. Only one is shown here for simplicity.

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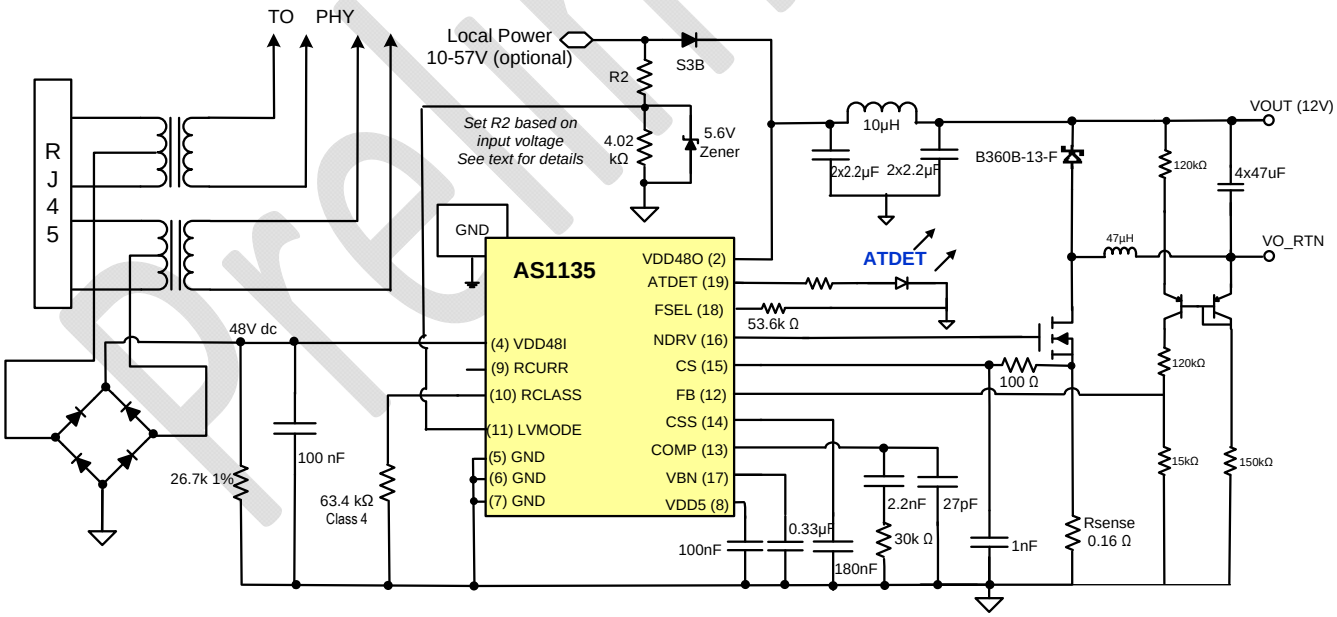
Figure 9: PoE PD Controller with Non-Isolated BUCK DC-DC converter (Conceptual Schematic)

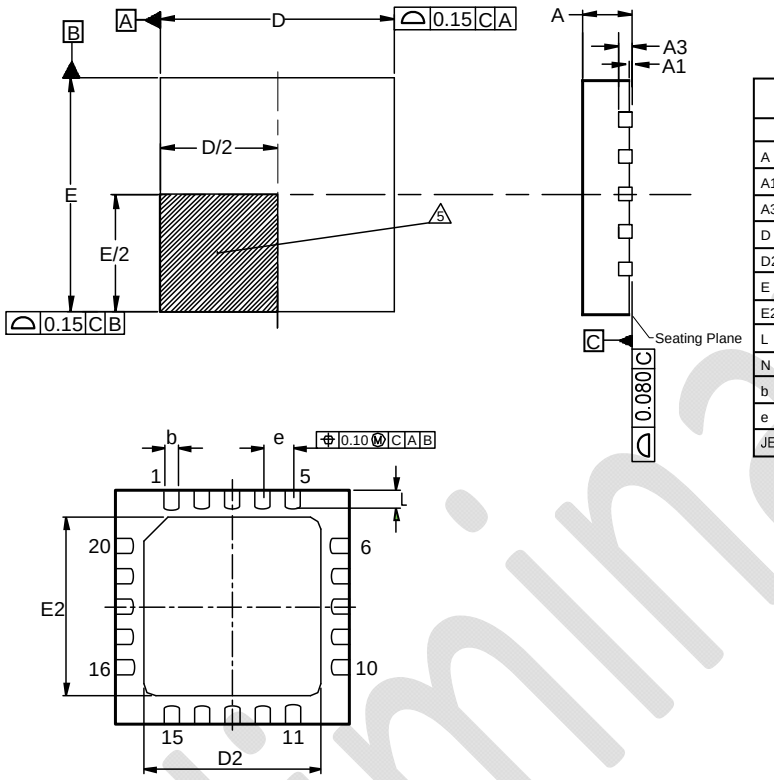


Notes:

This is a simplified conceptual schematic. Please refer to the reference design documentation for detailed design and component information. Full PoE implementation will require 2 input diode bridges. Only one is shown here for simplicity.

PHYSICAL DIMENSIONS

20 Pin QFN Package, 5mm X 5mm



Common Dimensions			
	MIN.	NOM.	MAX
A	0.80	0.85	0.95
A1	0.00	0.02	0.04
A3		0.20 REF.	
D	4.85	5.00	5.15
D2	3.70	3.80	3.90
E	4.85	5.00	5.15
E2	3.70	3.80	3.90
L	0.35	0.40	0.45
N		20L	
b	0.25	0.30	0.35
e		0.650 BSC	
JEDEC		MO-220-VHHC-2	

NOTES
1. Controlling dimensions in mm.
2. Dimension tolerances are ±0.1 (angular tolerance ±3°) unless otherwise specified.
3. All dimensions and tolerances conform to ANSI Y14.5M-1994.
4. Coplanarity applies to exposed pad as well as the terminals.
5. Pin 1 location may be identified by either a mold or marked feature.
6. JEDEC reference MO-220.

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