2M8-MOD-SRAM
REV. 1.0.0
January 05, 2001

Description

JSSM2MX8 is a 16 Megabit CMOS Static RAM Module based on four 512Kx8 Static RAMs mounted on a multi-layered epoxy laminate (FR4) substrate.

The JSSM2MX8 is offered on a double sided, 36 pin single-inline package (SIP), which provides a cost effective solution to very high packing density.

The Static RAMs employed are of Hi-CMOS process technology which helps realise higher density, higher performance and low power consumption.

All inputs and outputs are TTL compatible and operate from a single 5V power supply.

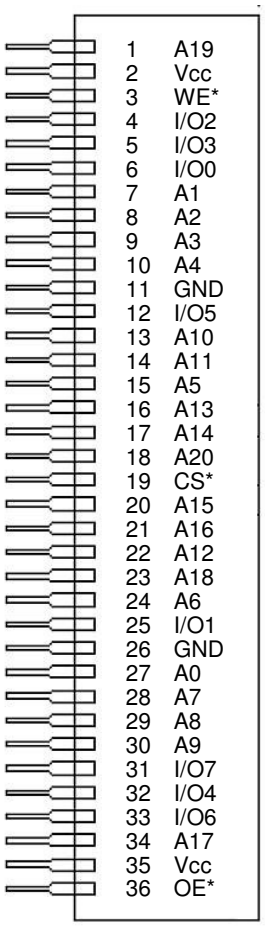
The JSSM2MX8 is fully asynchronous and completely static. No clocks or timing strobe is required for operation.

Features

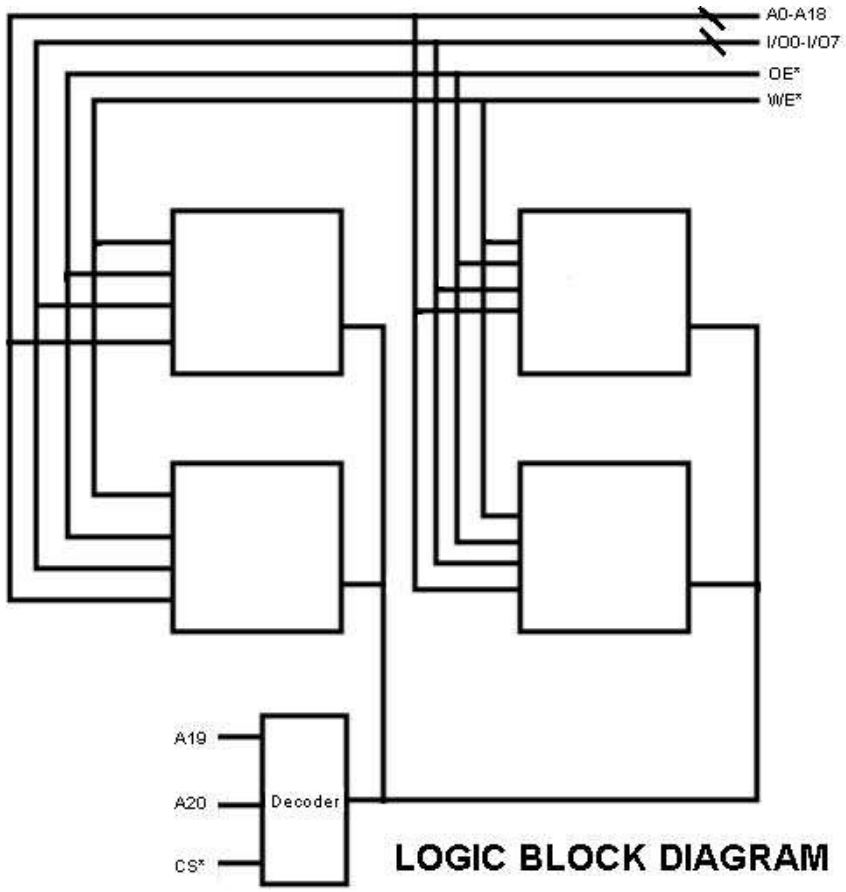
- 2 Meg x 8 bit CMOS Static
- Single 5V supply
- Access Time : 55/70 ns (max)
- Directly TTL compatible : All inputs and outputs
- Completely Static memory. No clock or timing strobe required
- 36 Pin Single-in-line Package

Ordering Information

Device	Package	Shipping Information	
JSSM2MX8-70	SIP-36	25 Units per tray	100 Units Per Box
JSSM2MX8-55	SIP-36	25 Units per tray	100 Units Per Box



PIN CONFIGURATION



LOGIC BLOCK DIAGRAM

Pin Description

Pin Name	Function
A0 – A20	Address Input
I/O0 – I/O7	Data Input/Output
CS*	Chip Select
OE*	Output Enable
WE*	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No connection

Function Table

WE*	CS*	OE*	Mode	V_{CC} Current	Dout pin	Ref. Cycle
x	H	x	Not Selected	I_{SB}, I_{SB1}	High-Z	-
H	L	H	Output Disable	I_{CC}	High-Z	-
H	L	L	Read	I_{CC}	Dout	Read Cycle
L	L	x	Write	I_{CC}	Din	Write Cycle

Note : x : H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage	V_{CC}	-0.5 to +7.0	V
Voltage on any pin relative to V_{SS}	V_T	-0.5[*1] to V_{CC} + 0.3[*2]	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	-20 to +70	^{O}C
Storage temperature	Tstg	-55 to +125	^{O}C
Storage temperature under bias	Tbias	-20 to +85	^{O}C

Notes : 1. V_T min: -3.0V for pulse half-width ≤ 30 ns.
2. Maximum voltage is 7.0 V.

Recommended DC Operating Conditions (Ta = -20 to +70 ^{O}C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.2	-	V_{CC} + 0.3	V
Input low voltage	V_{IL}	-0.3[*1]	-	0.8	V

Notes : 1. V_{IL} min: -3.0V for pulse half-width ≤ 30 ns.

DC Characteristics (Ta = -20 to +70 ^{O}C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	-20	-	+20	µA	Vin = V_{SS} to V_{CC}
Output leakage current	I_{LO}	-20	-	+20	µA	$V_{I/O}$ = V_{SS} to V_{CC}
Operating power supply current: DC	I_{CC}	-	-	110	mA	CS* ≤ V_{IL}, $I_{I/O}$ = 0mA, min. cycle
Standby power supply current: DC	I_{SB}	-	-	64	mA	CS* ≥ V_{IH}
Standby power supply current (1): DC	I_{SB1}	-	-	20	mA	Vin ≥ V_{CC} – 0.2V or Vin ≤ 0.2V, CS* ≥ V_{IH}
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -1.0 mA

Notes :1. Typical values are at V_{CC}=5.0V, Ta=+25^{O}C and specified loading and not guaranteed

Capacitance (Ta = +25 ^{O}C, f = 1 MHz, V_{CC} = 5.0 V)

Parameter	Symbol	Max	Unit
Input Capacitance*1 (A0–A16, OE*, WE*)	C_{IN1}	120	PF
Input Capacitance*1 (A17–A20, CS*)	C_{IN2}	25	PF
Output Capacitance*1	C_{OUT}	160	PF

Notes :1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta= -20 to +70^{O}C, V_{CC}= 5.0 V±10% unless otherwise noted)

Test Conditions

- Input pulse levels : 0.8 V to 2.4 V
- Input rise and fall times : 5 ns
- Input and output timing reference levels : 1.5 V
- Output load : 1 TTL Gate + C_L (100pF)
  (Including Scope and Jig)

Read Cycle

		-55 ns		-70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read cycle time	t_{RC}	55	-	70	-	ns	
Address access time	t_{AA}	-	55	-	70	ns	
Chip select access time	t_{CO}	-	55	-	70	ns	
Output enable to output valid	t_{OE}	-	25	-	35	ns	
Chip selection to output in low-Z	t_{LZ}	10	-	10	-	ns	2
Output enable to output in low-Z	t_{OLZ}	5	-	5	-	ns	2
Chip deselection to output in high-Z	t_{HZ}	0	20	0	25	ns	1, 2
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	ns	1, 2
Output hold from address change	t_{OH}	10	-	10	-	ns	

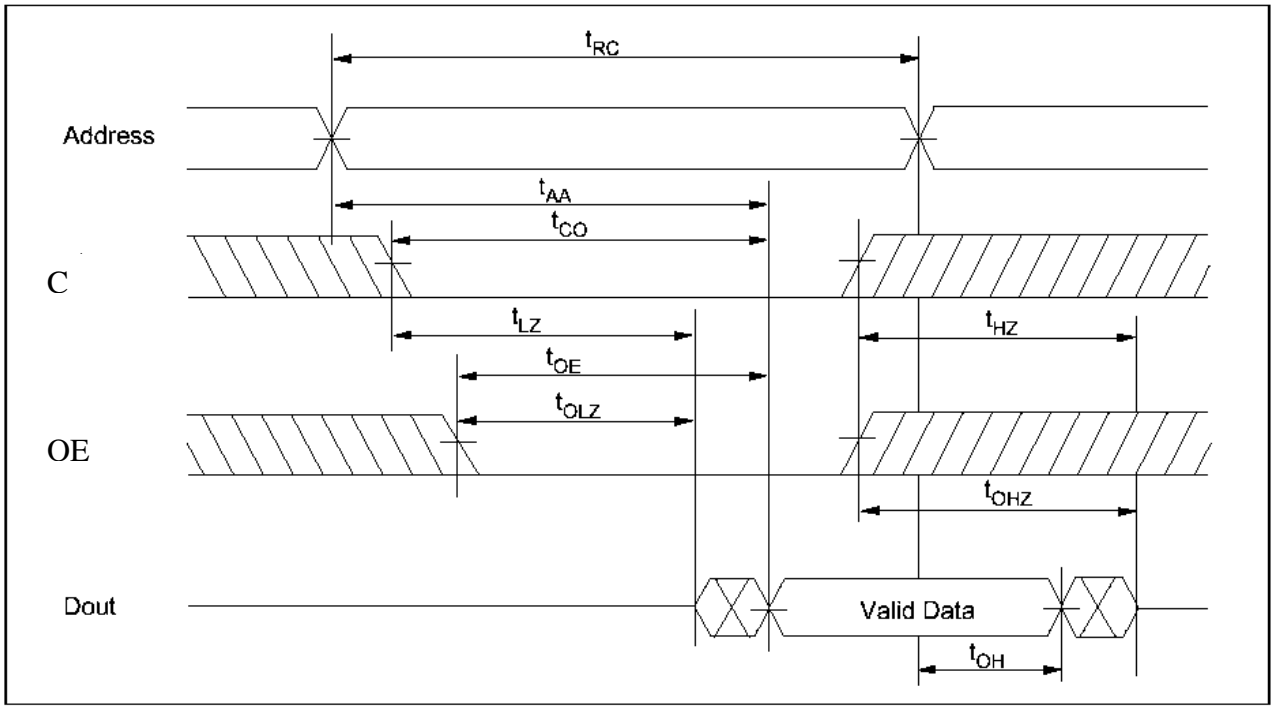
Write Cycle

		-55 ns		-70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write cycle time	t_{WC}	55	-	70	-	ns	
Chip selection to end of write	t_{CW}	50	-	60	-	ns	4
Address setup time	t_{AS}	0	-	0	-	ns	5
Address valid to end of write	t_{AW}	50	-	60	-	ns	
Write pulse width	t_{LZ}	40	-	50	-	ns	3, 12
Write recovery time	t_{WR}	0	-	0	-	ns	6
WE* to output high-Z	t_{WHZ}	0	20	0	25	ns	1, 2, 7
Data to write time overlap	t_{DW}	25	-	30	-	ns	
Data hold from write time	t_{DH}	0	-	0	-		
Output active from output in high-Z	t_{OW}	5	-	5	-		2
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	ns	1, 2, 7

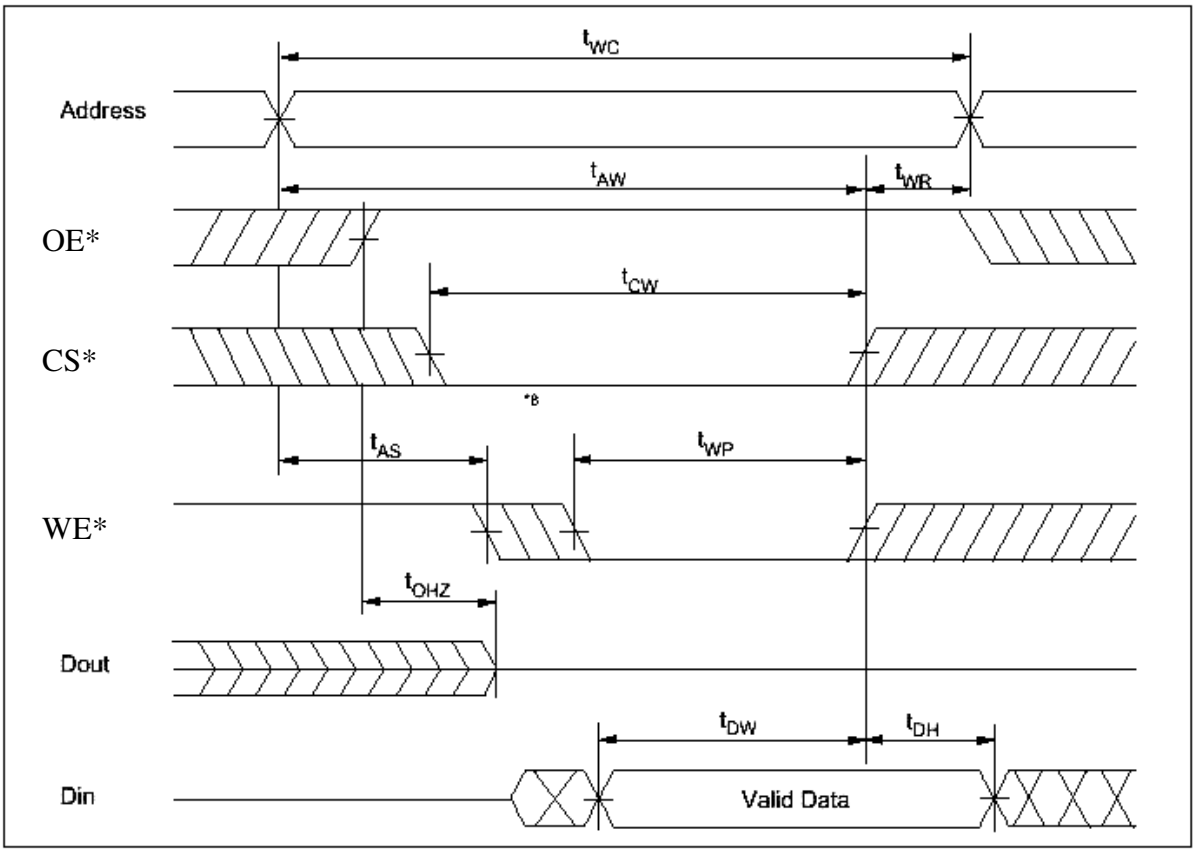
Notes :1. t_{HZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are referred to output voltage levels.
2. This parameter is sampled and not 100% tested
3. A write occurs during the overlap (t_{WP}) of a low CS* and a low WE*. A write begins at the later transition of CS* going low or WE* going low. A write ends at the earlier transition of CS* going high or WE* going high. t_{WP} is measured from the beginning of the write to the end of the write.
4. t_{CW} is measured from CS* going low to the end of write.
5. t_{AS} is measured from the address valid to the beginning of the write.
6. t_{WR} is measured from the earlier of WE* or CS* going high to the end of write cycle.
7. During this period, I/O pins are in the output state so that the output signals in the opposite phase to the outputs must not be applied.
8. If the CS* low transition occurs simultaneously with the WE* low transition or after the WE* transition, the output remain the in high impedance state.
9. Dout is the same phase of the write data of this write cycle.
10. Dout is the read data of next address.
11. If CS* is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
12. In the write cycle with OE* low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus retention. $t_{WP} \geq t_{DW}$ min + t_{WHZ} max.

Timing Waveforms

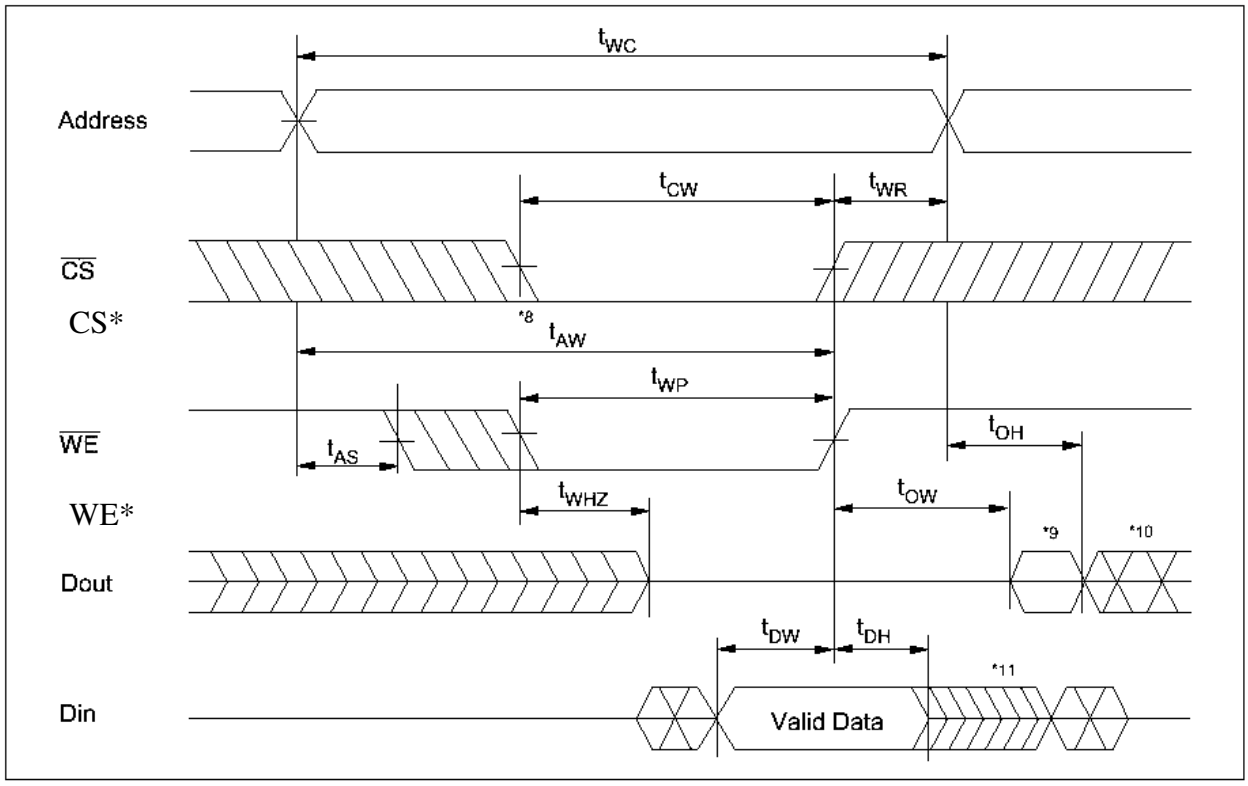
Read Timing Waveform ($WE^* = V_{IH}$)



Write Timing Waveform (1) (OE* Clock)



Write Timing Waveform (2) (OE* Low Fixed)

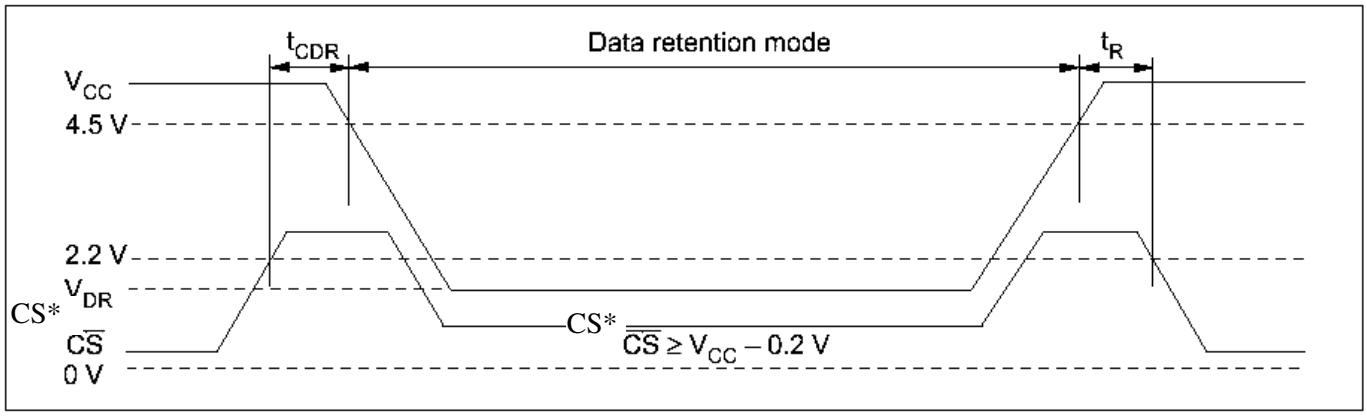


Low V_{CC} Data Retention Characteristics (Ta = -20 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions*2
V_{CC} for data retention	V_{DR}	2	-	-	V	CS* ≥ V_{CC} – 0.2 V, Vin ≥ 0 V
Data retention current	I_{CCDR}	-	1*3	350*1	µA	V_{CC} = 3.0 V, Vin ≥ 0 V CS* ≥ V_{CC} – 0.2 V
Chip deselect to data retention time	t_{CDR}	0	-	-	Ns	See retention waveform below
Operation recovery time	t_R	t_{RC}*4	-	-	Ns	

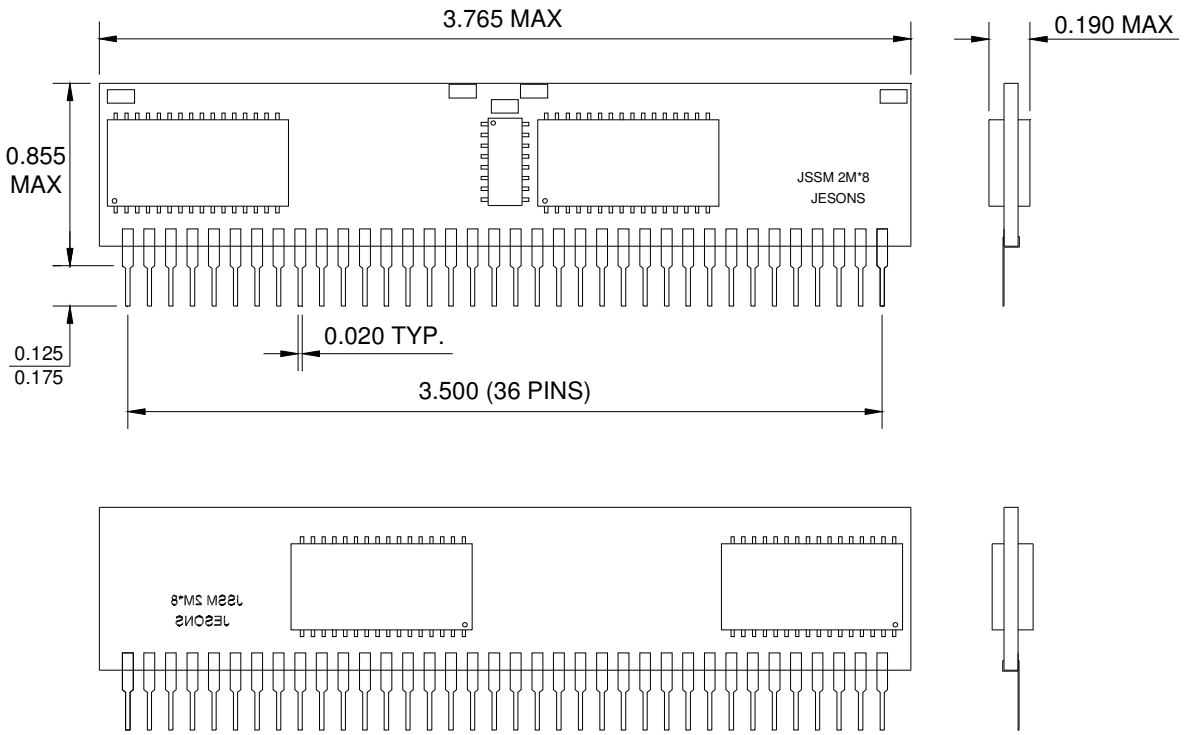
Notes : 1. For L-version (standard) at Ta = -20 to +40 °C.
2. CS* controls address buffer, WE* buffer, OE* buffer, and Din buffer. In data retention mode, Vin levels (address, WE*, OE*, I/O) can be in the high impedance state.
3. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and specified loading, and not guaranteed.
4. t_{RC} = read cycle time

Low V_{CC} Data Retention Timing Waveform (CS* controlled)



Package Description

(Dimensions in inches)



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